## REMARKS

Claims 1, 2, 6, 7, 9, 13, 14, 16, 17, 20, 25, and 27-38 are pending. Claims 1, 6, 7, 10, 11, 14, 16, 20, 25, and 30 have been amended, claims 3-5, 8, 12, 15, 18, 19, 21-24, and 26 have been canceled, and new claims 36-38 have been added to recite additional features of the embodiments disclosed in the specification.

## I. The First § 103 Rejection

In the Office Action, claims 1-5, 10, 14, 16, 18, 20 and 29-34 were rejected for being obvious in view of a Desprez-Rajashekara combination. This rejection is traversed for the following reasons.

### A. Claim 1 and its Dependent Claims

Claim 1 recites an extractor to extract energy from the ultracapacitor. The extractor includes a first amplifier circuit, a divider, and a controller which perform specific functions not taught or suggested by the Desprez and Rajashekara references, whether taken alone or in combination.

The Desprez publication discloses a circuit which recharges a supercapacitor when the voltage stored in the supercapacitor falls below a predetermined level. In contrast, the system of claim 1 does not recharge its ultracapacitor. Rather, the system of claim 1 amplifies the remaining output voltage of the ultracapacitor when the voltage stored in the ultracapacitor is detected to fall below a first predetermined voltage of a load.

Based on these differences, Applicants submit that the Desprez publication does not teach or suggest the first amplifier circuit of claim 1, or any of the other features included in the extractor defined in this claim.

The Rajashekara publication discloses a power converter 11 which boosts the output voltage of an ultracapacitor in order to achieve a desired level. (See Paragraphs [22]-[26]). However, the Rajashekara publication does not teach or suggest an extractor as defined by the amendments to claim 1.

More specifically, the Rajashekara publication discloses a switch network 24 which transfers voltage from a battery $12_2$ to charge another ultracapacitor $12_3$ when the voltage level of the battery falls below the voltage level of the ultracapacitor. The switch network is switched according to the timing table shown in Table 2, and charging takes place through a inductors 32 and 34.

The Rajashekara publication, however, does not teach or suggest the following features of the extractor defined in claim 1: "a divider to divide the amplified voltage to form a first control signal for the first amplifier circuit" and "a controller to generate a second control signal to vary a ratio of the divider, the varied ratio adjusting the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage of the load." (See, for example, Figure 17 of the application drawings and corresponding portions of the specification for support).

Applicants submit that amended claim 1 and its dependent claims are allowable based on these differences.

Dependent claim 2 recites that the first amplifier circuit amplifies the output voltage of the ultracapacitor "when the detected voltage of the ultracapacitor is above a second predetermined voltage of the first amplifier circuit," and claim 30 recites that "the second predetermined voltage corresponds to a minimum operating voltage of the amplifier circuit." These feature are not taught or suggested by the Desprez and Rajashekara publications, whether taken alone or in combination.

Moreover, in the Final Office Action the Examiner indicated that the Desprez publication discloses the features of claim 30 in Paragraphs [20]-[25]. However, these paragraphs merely disclose how a charger is controlled to recharge an ultracapacitor. As acknowledged in the Office Action, the Desprez publication does not disclose the first amplifier circuit of base claim 1, as the newly cited Rajashekara publication was relied on to provide this feature.

It therefore logically follows that all features relating to generating the amplified ultracapacitor output by controlling the first amplifier circuit of claim 1, including the divider circuit and the controller recited in this claim, are missing from the Desprez publication. The Rajashekara publication is also deficient in this respect.

Applicants therefore submit that claim 30 is allowable, not only based on the features recited in claim 1 but also based on the features separately recited therein.

**B. Claim 10 and Its Dependent Claims**

Claim 10 has been amended to recite an extactor which includes "an adiabatic amplifier to amplify voltage output from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor." Claim 10 further recites that the adiabatic amplifier includes "first and second transmission gates that are alternatively switched to output an amplified differential signal that corresponds to the amplified voltage of the ultracapacitor." (See, for example, Figure 21 and corresponding portions of the specification for support.)

In rejecting claim 10, the Examiner relied on the Desprez publication. However, Desprez does not teach or suggest an adiabatic amplifier having transmission gates for generating an amplified different signal as now defined in claim 10. Applicants submit that claim 10 and its dependent claims are allowable based on these differences.

Claim 14 has been amended to recite features analogous to those which patentably distinguish claim 1 from the cited references, e.g., claim 14 recites "dividing the amplified voltage using a divider to form a first control signal for the first amplifier circuit" and "generating a second control signal to vary a ratio of the divider, the varied ratio adjusting the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage of the load." The Desprez and Rajashekara publications do not teach or suggest these features. Accordingly, it is submitted that claim 14 and its dependent claims are allowable.

Dependent claim 16 recites that "the varied ratio adjusts the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage during a time when the detected voltage of the ultracapacitor is above a second predetermined voltage of an amplifier circuit that is to perform said amplifying." The Desprez and Rajashekara publications do not teach or suggest these features, and neither do any of the other cited references.

## II. The Second § 103 Rejection

Claims 6, 12, 17, and 35 were rejected for being obvious based on a Desprez-Sasaki combination. This rejection is traversed on grounds that the Sasaki patent does not teach or suggest the features of base claims 1 and 14 missing from the Desprez publication.

That is, the Sasaki patent discloses adding voltage to the output of a chemical cell when the voltage stored in the chemical cells falls below a certain level. The Sasaki patent, however, does not teach or suggest an extractor for an ultracapacitor which includes "a first amplifier circuit to amplify an output voltage from the ultracapacitor when the detected voltage falls below a first predetermined voltage of a load coupled to the ultracapacitor," "a divider to divide the amplified voltage to form a first control signal for the first amplifier circuit," and "a controller to generate a second control signal to vary a ratio of the divider, the varied ratio adjusting the first control signal to maintain the output voltage of the ultracapacitor substantially equal to or above the first predetermined voltage of the load."

Based on these differences, it is respectfully submitted that claims 6, 17, and 35 are allowable.

## III. The Third § 103 Rejection

Claims 7 and 13 were rejected for being obvious in view of a Desprez-Bhowmik combination. This rejection is traversed for the following reasons.

Claim 7 recites an extractor to extract energy from the ultracapacitor when an output voltage of the ultracapacitor falls below a first predetermined voltage of a load. This extractor includes "a first capacitor to charge the ultracapactor to an output voltage during a charging cycle" and "a second capacitor that is to be coupled with the first capacitor during a discharging cycle while the first capacitor remains coupled to the ultracapacitor, the second capacitor being charged to a predetermined level based on a sum of a charge stored in the first capacitor and a charge stored in the ultracapacitor during said discharging cycle." (See, for example, the embodiment shown in Figure 19 and corresponding portions of the specification).

The Desprez publication does not disclose the particular features of the extractor of claim 7. To make up for these deficiencies, the Bhowmik patent was cited.

The Bhowmik patent discloses a switch controller 20 which selectively transfers energy to a load 110 from one or more of energy storage elements 80, 90, and 100, which are shown in the form of capacitors. The switching configuration of these energy sources may change depending on the needs of the load and/or when the monitored voltage in primary storage element 80 falls too low.

However, the Bhowmik patent does not teach or suggest a first capacitor to charge the ultracapactor to an output voltage during a charging cycle and a second capacitor that is to be coupled with the first capacitor during a discharging cycle while the first capacitor remains coupled to the ultracapacitor, the second capacitor being charged to a predetermined level based on a sum of a charge stored in the first capacitor and a charge stored in the ultracapacitor during said discharging cycle.

In the Final Office Action, the Examiner indicated that capacitor 80 corresponds to the first capacitor of claim 7 and capacitor 100 corresponds to the second capacitor. However, Bhowmik does not teach or suggest that capacitor 80 charges an ultracapactor to an output voltage during a charging cycle and that capacitor 100 that is to be coupled with the capacitor 80 during a discharging cycle while the first capacitor remains coupled to the ultracapacitor. Moreover, the Bhowmik patent discloses that capacitor 100 is the ultracapacitor, not the second capacitor of claim 7. (See column 6, lines 9-10).

The Bhowmik patent also does not teach or suggest that second capacitor 100 is charged to a predetermined level based on a sum of a charge stored in first capacitor 80 and a charge stored in the ultracapacitor during said discharging cycle. Rather, Bhowmik discloses that capacitor 100 is charged based on an auxiliary current 360 which does not correspond to a voltage equal to the "sum" recited in claim 7. (See column 12, lines 30-45).

Based on the foregoing differences, it is submitted that claim 7 and its dependent claims are allowable.

## IV. The Fourth § 103 Rejection

Claims 9 and 11 were rejected for being obvious in view of a Desprez-Williams combination. This rejection is traversed on grounds that the Williams patent does not teach or suggest the features of base claims 7 and 10 missing from the Desprez publication.

## V. The Fifth § 103 Rejection

Claims 25, 27, and 28 were rejected for being obvious in view of a Sasaki-Rejashekara combination. This rejection is traversed on grounds that the Sasaki patent and Rajashekara publication do not teach or suggest the features added by amendment to base claim 25, which features correspond to those that patentably distinguish claim 1 from the aforementioned references.

## VI. New Claims

New claims 36-38 have been added to the application.

Claim 36 recites that the divider of claim 1 "includes a network of variable resistors." These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 37 recites that the second control signal of claim 1 "is to vary values of the variable resistors to change amplification of the first amplifier circuit, the changed amplification causing the output voltage of the ultracapacitor to be substantially equal to or above the first predetermined voltage of the load." (See, for example, page 21 of the specification for support).

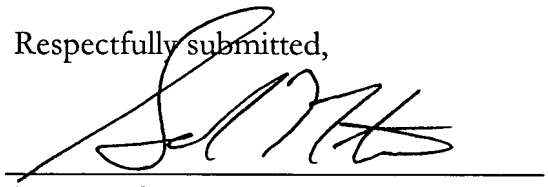
These features are not taught or suggested by the cited references, whether taken alone or in combination.

Claim 38 recites that "the ratio of the divider is continuously changed by the controller as the detected voltage of the ultracapacitor changes over time." (See, for example, page 21 of the specification for support). These features are not taught or suggested by the cited references, whether taken alone or in combination.

In view of the foregoing amendments and remarks, it is respectfully submitted that the application is in condition for allowance. Favorable consideration and timely allowance of the application is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this, concurrent and future replies, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,



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